

8. The semiconductor device of claim 1, wherein the second top surface is higher than the first top surface, and
the second electrode is between protruding portions of the second insulation above the first insulation pattern.
- 9-10. (canceled)
11. The semiconductor device of claim 1, further comprising:
a second conductive pattern on the second electrode, wherein
the second conductive pattern has a resistance lower than a resistance of the second electrode, and
the second conductive pattern extends in the second direction.
- 12-13. (canceled)
14. The semiconductor device of claim 1, wherein the variable resistance pattern includes a chalcogenide-based material.
15. The semiconductor device of claim 1, wherein the second electrode has a pillar shape.
16. The semiconductor device of claim 1, wherein the first and second top surfaces are substantially coplanar with each other, and
the second electrode is on the variable resistance pattern in the opening defined the first and second insulation patterns.
17. (canceled)
18. The method of claim 1, wherein an upper width in the second direction of the first conductive line is substantially the same as a lower width in the second direction of the first structure.
19. A semiconductor device, comprising:
a substrate;
a plurality of first conductive lines on the substrate, the first conductive lines extending in a first direction;
a plurality of first structures on the first conductive lines, the first structures being spaced apart from each other, the first structures including a switching pattern and a first electrode sequentially stacked, and top surfaces of the switching pattern and the first electrode being substantially coplanar with each other;
a first insulation pattern on the substrate, the first insulation pattern extending in the first direction to fill a space between the first structures in a second direction that is substantially perpendicular to the first direction, and a first top surface of the first insulation pattern being higher than a top surface the first structures;
a second insulation pattern on the substrate, the second insulation pattern extending in the second insulation pattern to fill a space between the first structures in the first direction, and the second insulation pattern having a second top surface that is higher than a top surface of the first structures;
a first spacer on upper sidewalls of the first insulation pattern above the first structures;
a second spacer on upper sidewalls of the second insulation pattern above the first structures;
a variable resistance pattern on the first structures, the variable resistance pattern filling an opening defined by the first and second insulation patterns; and
a second electrode on the variable resistance pattern.
20. The semiconductor device of claim 19, wherein the second electrode extends in the second direction.
21. The semiconductor device of claim 19, wherein the second electrode has a pillar shape.
22. The semiconductor device of claim 19, wherein the variable resistance pattern includes a chalcogenide-based material.
- 23-35. (canceled)
36. A semiconductor device, comprising:
a substrate;
first conductive lines on the substrate, the first conductive lines extending in a first direction and being spaced apart from each other in a second direction that intersects the first direction;
first structures on the first conductive lines, the first structures being spaced apart from each other in the first direction on the first conductive lines;
a variable resistance pattern on the first structures, the variable resistance pattern including variable resistance structures on the first structures, respectively;
electrodes on the substrate over the variable resistance pattern, the electrodes being spaced apart from each other in the first direction and extending in the second direction, the electrodes crossing over the first conductive lines;
a first insulation pattern on the substrate, the first insulation pattern extending between a bottom surface of the electrodes and a portion of the substrate exposed by the first conductive lines; and
a second insulation pattern on the first conductive lines, the second insulation pattern extending in the second direction, the second insulation pattern extending between adjacent pairs of the first structures, between adjacent pairs of the variable resistance structures, and between adjacent pairs of the electrodes.
37. The semiconductor device of claim 36, further comprising:
first spacers on the first structures; and
second spacers on the first structures, wherein
the first structures include a first electrode on a switching structure,
the electrodes on the substrate over the variable resistance pattern are second electrodes,
there are two of the first spacers spaced apart from each other in the second direction on each of the first structures,
there are two of the second spacers spaced apart from each other in the first direction on each of the first structures, the variable resistance structures on the first structures are between the two of the first spacers and the two of the second spacers, and
a height of the second spacers is greater than a height of the first spacers.
38. The semiconductor device of claim 36, wherein an area of a bottom of the variable resistance structures is less than an area of a top of the variable resistance structures.
39. The semiconductor device of claim 36, wherein
the first insulation pattern extends between adjacent pairs of the first conductive lines, and
a bottom surface of the first insulation pattern is closer to the substrate than a bottom surface of the second insulation pattern.
40. The semiconductor device of claim 36, wherein a top surface of the second insulation pattern is level with a top surface of the electrodes.